Notice of References Cited	Application/Control No. 10/007,007	Applicant(s)/Patent Under Reexamination WHEELER ET AL.	
	Examiner Russell L. Guill	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,195,627	02-2001	Bargh et al.	703/14
*	B	US-6,470,478	10-2002	Bargh et al.	716/4
*	C	US-6,920,418	07-2005	Roesner et al.	703/17
*	D	US-6,978,231	12-2005	Williams et al.	703/14
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	K.F. Wong et al.; "Statistics on Logic Simulation", 1986, IEEE 23rd Design Automation Conference
	V	Mani B. Srivastava et al.;"Using VHDL for High-Level, Mixed-Mode System Simulation", September 1992, IEEE Design & Test of Computers, Volume 9, Issue 3
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.